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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,813	01/06/2006	Hidehiko Shoji	P29099	1906

52123 7590 04/10/2009

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EXAMINER	
WILLIS, RANDAL L	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
04/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/563,813	SHOJI ET AL.	
	Examiner	Art Unit	
	RANDAL WILLIS	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-22* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/6/06, 7/19/07, 11/06/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10563813 filed January 6th 2006. Claims 1-22 are currently pending and have been examined.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on April 6th 2006, July 19th 2007 and November 6th 2007 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 13-15, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwami (2002/047575) in view of Nakamura (2001/0024179).

Apropos claim 1, Iwami teaches:

A display device comprising:

first electrodes classified into a plurality of groups (Z1-Zm, Fig. 3);

second electrodes respectively provided so as to cross said first electrodes (X1-Xn);

a display panel having a plurality of capacitive light emitting elements respectively provided at intersections of said first electrodes and said second electrodes (Plasma display pixels are inherently capacitive light emitting elements); and

a recovering capacitive element (C1, Fig. 9);

an application circuit that discharges charges to said first electrodes from said recovering capacitive element or recovers the charges from said first electrodes in said recovering capacitive element, to apply a driving pulse for applying the data pulse to said first electrodes (energy recovery circuit 21, Fig. 9); and

a potential limiting circuit that limits a quantity of the charges recovered in said recovering capacitive element, to limit a potential of said recovering capacitive element so as not to exceed a predetermined value (23, Fig. 9, [0089]).

However, Iwami fails to explicitly teach:

a drive circuit that applies a data pulse for light-emitting the a selected capacitive light emitting element to the first electrodes in said plurality of groups such that phase differences respectively occur between said plurality of groups, said drive circuit comprising

In the same field of plasma display panels, Nakamura teaches dividing the data electrodes into different groups (Da electrodes and Db electrodes, FIg. 8) and a phase control circuit to create a phase difference between the two groups of electrodes ([0080] and Fig. 9).

Therefor it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the known driving method of Nakamura to the display device of Iwami in order to provide a display device that suppresses power consumption [0036].

Apropos claim 2, Iwami teaches:

A display device comprising:

first electrodes classified into a plurality of groups (Z1-Zm, Fig. 3);

second electrodes respectively provided so as to cross said first electrodes (X1-Xn);

a display panel having a plurality of capacitive light emitting elements respectively provided at intersections of said first electrodes and said second electrodes (Plasma display pixels are inherently capacitive light emitting elements); and

an inductive element (L1 and L2, Fig. 9);

a recovering capacitive element (C1, Fig. 9);

an application circuit that discharges charges to said first electrodes from said recovering capacitive element by a resonance operation of a capacitance of said display panel and said inductive element or recovers the charges in said recovering capacitive element from said first electrodes through said inductive element, to apply to a first node a driving pulse for applying a data pulse to the first electrodes in said plurality of groups (Energy recover 21, Fig. 9); and

a potential limiting circuit that limits a quantity of the charges recovered in said recovering capacitive element, to limit a potential of said recovering capacitive element so as not to exceed a predetermined value (23, Fig. 9, [0089]).

However, Iwami fails to explicitly teach:

a drive circuit that applies a data pulse for light-emitting the a selected capacitive light emitting element to the first electrodes in said plurality of groups such that phase differences respectively occur between said plurality of groups, said drive circuit comprising

In the same field of plasma display panels, Nakamura teaches dividing the data electrodes into different groups (Da electrodes and Db electrodes, FIg. 8) and a phase

control circuit to create a phase difference between the two groups of electrodes ([0080] and Fig. 9).

Therefor it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the known driving method of Nakamura to the display device of Iwami in order to provide a display device that suppresses power consumption [0036].

Apropos claim 3 and 19, Iwami teaches:

A display device, comprising:

first electrodes classified into a plurality of groups (Z1-Zm, Fig. 3);

second electrodes respectively provided so as to cross said first electrodes (X1-Xn);

a display panel having a plurality of capacitive light emitting elements respectively provided at intersections of said first electrodes and said second electrodes (Plasma display pixels are inherently capacitive light emitting elements); and

a first power supply terminal that receives a first power supply voltage (V1, Fig. 9);

an inductive element (L1 and L2, Fig. 9);

a recovering capacitive element (C1, Fig. 9);

an application circuit that discharges charges from said recovering capacitive element by a resonance operation of a capacitance of said display panel (21, Fig. 9) and said inductive element to raise a potential at a first node, connects said first node and said first power supply terminal to each other, then disconnects said first node and

said first power supply terminal from each other, and recovers the charges in said recovering capacitive element from said first node through said inductive element by said resonance operation to lower the potential at said first node, to apply to said first node a driving pulse for applying a data pulse to the first electrodes in said plurality of groups ([0052] and [0053]); and

a potential limiting circuit that limits a quantity of the charges recovered in said recovering capacitive element, to limit a potential of said recovering capacitive element so as not to exceed a predetermined value lower than said first power supply voltage (23, Fig. 9, [0089]).

However, Iwami fails to explicitly teach:

a drive circuit that applies a data pulse for light-emitting the a selected capacitive light emitting element to the first electrodes in said plurality of groups such that phase differences respectively occur between said plurality of groups, said drive circuit comprising

In the same field of plasma display panels, Nakamura teaches dividing the data electrodes into different groups (Da electrodes and Db electrodes, FIg. 8) and a phase control circuit to create a phase difference between the two groups of electrodes ([0080] and Fig. 9).

Therefor it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the known driving method of Nakamura to the display device of Iwami in order to provide a display device that suppresses power consumption [0036].

Apropos claim 13 and 22, Iwami teaches:

The display device according to claim 3, wherein said predetermined value is more than one-half said first power supply voltage and is not more than four-fifth said first power supply voltage (within the range set by Iwami [0088]).

Apropos claim 14, Iwami and Nakamura fail to explicitly teach:

wherein said phase difference is not less than 200 ns.

However, Nakamura teaches the phase difference can be change [0083] and therefore the arrival at 200ns would have be obvious to one of ordinary skill in the art at the time of the invention simply by performing optimization of the system taught by Nakamura.

Apropos claim 15, Nakamura teaches:

The display device according to claim 3, further comprising:

a plurality of drive circuits (20-1 and 20-2, Fig. 8);

said plurality of drive circuits being respectively provided in correspondence with said plurality of groups (Da for 20-1 and Db for 20-2, Fig. 8); and

said plurality of drive circuits respectively applying the data pulses for light-emitting the selected capacitive light emitting element to said first electrodes in said plurality of groups such that phase differences respectively occur between said plurality of groups (Drivers drive pixels 16, Fig. 8).

6. Claims 4-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Iwami and Nakamura as applied to claim3 above, and further in view of Nagaoka (7,212,194).

Apropos claim 4, Iwami fails to teach:

The display device according to claim 3, wherein the inductive element is provided between said first node and a second node,

said recovering capacitive element is connected to a third node),

said potential limiting circuit limits a potential at said third node to limit the potential of said recovering capacitive element so as not to exceed said predetermined value

said application circuit comprising:

a first switching element provided between said first power supply terminal and said first node;

a second switching element provided between a ground terminal receiving a ground potential and said first node;

a third switching element provided between said second node and said third node, wherein

a fourth switching element provided between said second node and said third node, and

in an address time period during which said selected capacitive light emitting element in said display panel is to be light-emitted, the third switching element is turned on so that the charges are discharged into said first node from said recovering capacitive element through said inductive element, the potential at said first node is raised, said third switching element is turned off and said first switching element is turned on so that the potential at said first node is raised to said first power supply voltage, and said first switching element is turned off and said fourth switching element is turned on so that the charges are recovered in said recovering capacitive element from said first node through said inductive element so that the potential at said first node is lowered, thereby generating said driving pulse.

However, in the same field of energy recovery circuits, Nagaoka teaches an energy recovery circuit (Fig. 5) which contains a first node (connection of L and 2) a second node (Connection of L, D1 and D2) and a third node (connection of C1, S1 and S2), an inductor (L), a first power supply (B1), a first switch (S3), a second switch (S4), a third switch (S1) and a fourth switch (S2). The operation of this circuit is described in Col 6 lines 9-65 and aligns with the procedure claimed above.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known energy recovery technique taught by Nagaoka, to replace the energy recovery circuit 21 of Iwami to achieve the predictable result of an energy recovery circuit to conserve power in the plasma display panel.

Apropos claim 5, Nagaoka further teaches:

wherein said drive circuit further comprises first switching circuits respectively provided in correspondence with said first electrodes (22, Fig. 5), and is operated such that;

said first switching circuit is turned on so that the charges are recovered and discharged between said first node and said first electrode, and said first switching circuit is turned off so that said corresponding first electrode is set to the ground potential (Switches switch between ground and energy recovery circuit 21 Fig. 5).

Apropos claim 6, Iwami teaches:

The display device according to claim 4, wherein said potential limiting circuit comprises:

a division circuit that divides a voltage between said first power supply voltage and a ground potential to produce a potential approximately equal to said predetermined value (Resistors R2 and R3, Fig. 9); and

a second switching circuit connected between said third node and said ground terminal and receiving the potential produced by said division circuit as a control signal, and turned on when the potential at said third node exceeds said predetermined value (Q1 receives predetermined value based on voltage division across R2 and R3, Fig. 9).

Apropos claim 7, Iwami teaches:

The display device according to claim 4, wherein said potential limiting circuit comprises:

a second power supply terminal receiving a second power supply voltage approximately equal to said predetermined value (Vref, Fig. 9); and

a second switching circuit connected between said third node and said ground terminal and receiving said second power supply voltage received by said second power supply terminal as a control signal, and turned on when the potential at said third node exceeds said predetermined value (Q1 and D3, Fig. 9).

Apropos claim 8, Iwami teaches:

The display device according to claim 6, wherein said second switching circuit comprises:

a unidirectional conductive element provided between said third node and a fourth node and causing a current to flow from said third node to said fourth node (D3, Fig. 9); and

a fifth switching element provided between said fourth node and said ground terminal, and having a control terminal receiving said control signal (Q1, Fig. 9).

Apropos claim 9, Iwami teaches:

The display device according to claim 4, wherein said potential limiting circuit comprises:

a unidirectional conductive element provided between said third node and said ground terminal and causing a current to flow from said third node to said ground

terminal when the potential at said third node exceeds said predetermined value (D3, Fig. 9).

Apropos claim 10, Iwami teaches:

The display device according to claim 9, wherein said unidirectional conductive element is a zener diode (D3, Fig. 9).

Apropos claim 11, Iwami and Nagoaka fails to explicitly teach:

The display device according to claim 4, further comprising a charge pump circuit that produces a potential higher than the potential at said first node in order to turn said first switching element on.

However, Examiner takes official notice that the use of charge pumps is well known in the art and thus would have been obvious to one of ordinary skill in the art at the time of the invention to use a charge pump to create a potential high enough to turn on the S3.

Apropos claim 12, Iwami and Nagoaka fail to explicitly teach:

wherein said charge pump circuit comprises:

a charging capacitive element provided between said first node and a fifth node;

a unidirectional conductive element provided between a third power supply terminal receiving a third power supply voltage and said fifth node and causing a current to flow from said second power supply terminal to said fifth node; and

a control signal output circuit that adds a potential at said fifth node to the potential at said first node, and outputs a potential obtained by the an addition to said first switching element as a control signal.

However, examiner takes official notice that charge pumps that are comprised of capacitors, diodes and switches between various power supplies are well known in the art and thus it would have been obvious to one of ordinary skill in the art at the time of the invention to employ the well known concept of a charge pump to create the necessary control signals for switch S3 of Nagoaka.

7. Claims 16, 18, 20 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Iwami and Nakamura as applied to claims 3 and 19 above, and further in view of Hoppenbrouwers (2005/0082957).

Apropos claim 16 and 20, Iwami and Nakamura fail to teach:

a number-of-times detector for detecting the number of times of rise or the number of times of fall of the data pulse applied to said first electrodes,

said drive circuit further comprising:

a controller for calculating the a ratio of said number of times detected by said number-of-times detector to a maximum number of times the data pulse can rise or the number of times the data pulse can fall, lowering, when said ratio is more than a predetermined ratio value, the potential at said first node to a predetermined voltage

value, and then controlling the operation of said application circuit such that said first node is grounded.

However, in the same field of plasma displays with energy recovery systems, Hopenbrouwers teaches determining the number of sustain pulses in a subfield, and only activating the energy recovery circuits for the subfields with lower sustain pulses in which the energy recover is higher than a break-even-point (Figures 9 and 10, [0061]).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Hoppenbrouwers into the plasma display of Iwami and Nakamura, in which grounding the first node would effectively prevent the energy recovery circuit from operating when the break-even point of sustain pulses has been reached in order to conserve power.

Apropos claims 18 and 21, Iwami, Nakamura and Hoppenbrouwers fail to explicitly teach:

Wherein said predetermined ratio value is not less than 95%

However, the exact ratio used is a matter of design choice and optimization values, and thus would be readily apparent to one of ordinary skill in the art at the time of the invention.

Allowable Subject Matter

8. Claim 17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RANDAL WILLIS whose telephone number is (571)270-1461. The examiner can normally be reached on Monday to Thursday, 8am to 5pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RLW

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629